Timing Architects

Model-Based Development Tools for Embedded Multi-Core Systems

"Multicore and multiprocessor software projects are 4.5x more expensive, have 25% longer schedules, and require almost 3x as many software engineers."[1]

Meet the Multi-Core Challenge

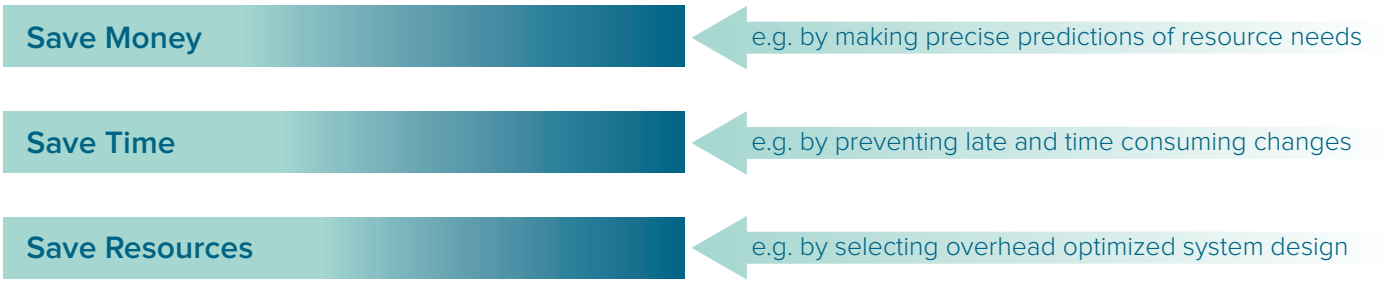
The demand for more sophisticated comfort features, and increasing safety requirements are factors that express the need for additional processing power within embedded systems. Due to physical restrictions, which limit further increases of clock rates, single-core processors are no longer adequate to satisfy the requirements of next generation embedded systems.

This makes changes towards a new processing technology with multi-core inevitable. Multi- and many-core processors will be the basis technology for future embedded systems as all leading chip manufacturers – Intel®, IBM®, ARM, Nvidia®, Freescale, MIPS, TI – are focusing their strategy on multi-core architectures[2].

Challenges due to the new Multi-Core technology

Surveys have shown, that using this new technology, multi-core and multi-processor software projects are 4,5 times more expensive, have 25% longer schedules, and require almost 3 times as many software engineers.

Master the Multi-Core Challenges with Timing Architects™



Timing-Architects™ Tool Suite enables engineers to master the multi-core challenges. By using TA tools for a multi-core project, costs, time, and the need of resources will be reduced and even drops below the level of expenses for a single-core project.

[1] VDC Research, "Next Generation Embedded Hardware Architectures: Driving Onset of Project Delays, Costs Overruns, and Software Development Challenges" – September 2010

[2] Arbeitskreis Multi-Core, Andreas Herkersdorf, TU Munich, Relevanz eines Multi-Core-Ökosystems für künftige Embedded Systems – December 2011

The Timing Architects™ Tool Suite

Integrated Solution for designing, developing and verifying embedded multi- and many-core systems

Closed-Loop Solution for iterative system design, simulation, automated optimization and target verification

Timing Architects™ Tool Suite Benefits

The TA Tool Suite is the framework of integrated development tools for real-time multi- and many-core systems. Regarding all these development steps the TA solution was especially designed for the embedded multi-core era.

Designer

- Specification of hierarchical requirements
- Design of software architectures
- Mapping of software functions to hardware resources
- Integration of new software modules in existing systems

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Simulator

- In-depth evaluation of the systems and components timing behavior
- Evaluation of hardware resource consumption of application software and operating system
- Performance analysis and evaluation of different hardware platforms and software designs
- Interference and cause-effect analysis
- Validation and comparison of design decisions early in the development process

Page 12

Optimizer

- Semi-automated design of embedded multi- and many-core software architectures
- Automated mapping of software functions to hardware resources
- Trade-off and capability analysis of embedded multi- and many-core software architectures as well as hardware platforms

Page 16

Inspector

- Verification of system implementations on target hardware
- Comparison of system implementations against simulation results and model specification
- Detection of hardware bottlenecks
- Reverse/re-engineering of legacy applications

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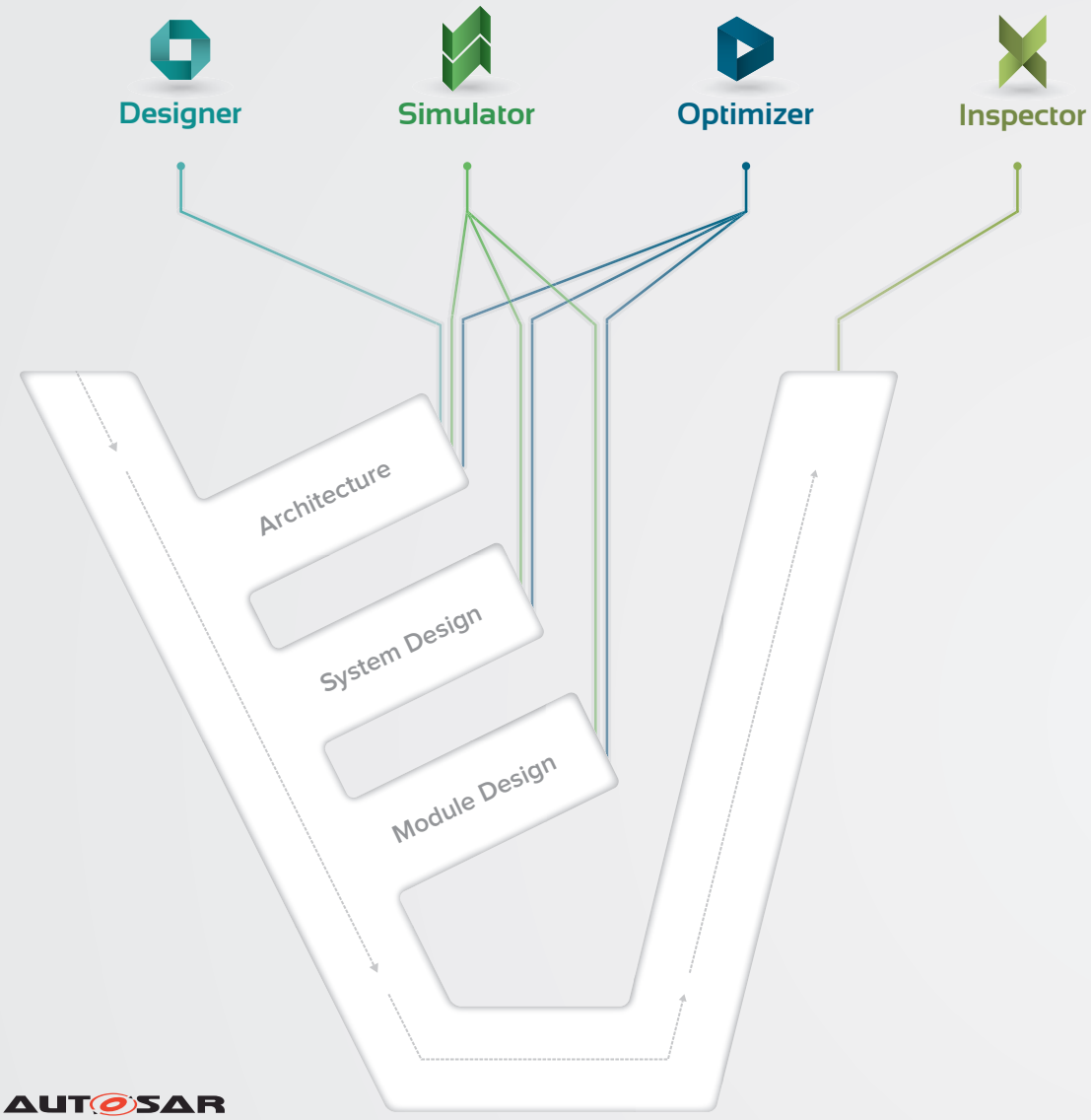
The Timing-Architects™ Tool Suite is a worldwide unique solution which covers the system design phase, simulation and analysis, architecture optimization and deployment, as well as target verification.

TA Tools in the Development Process

The integrated solution for designing, developing, and verifying embedded multi- and many-core systems – seamlessly integrated in your development process.



We are supporting AUTOSAR

The TA Tool Suite covers the whole development process of an embedded real-time system. With TA tools we support project managers, architects, developers, integration and test engineers alike to get the most out of the new multi-core technology.

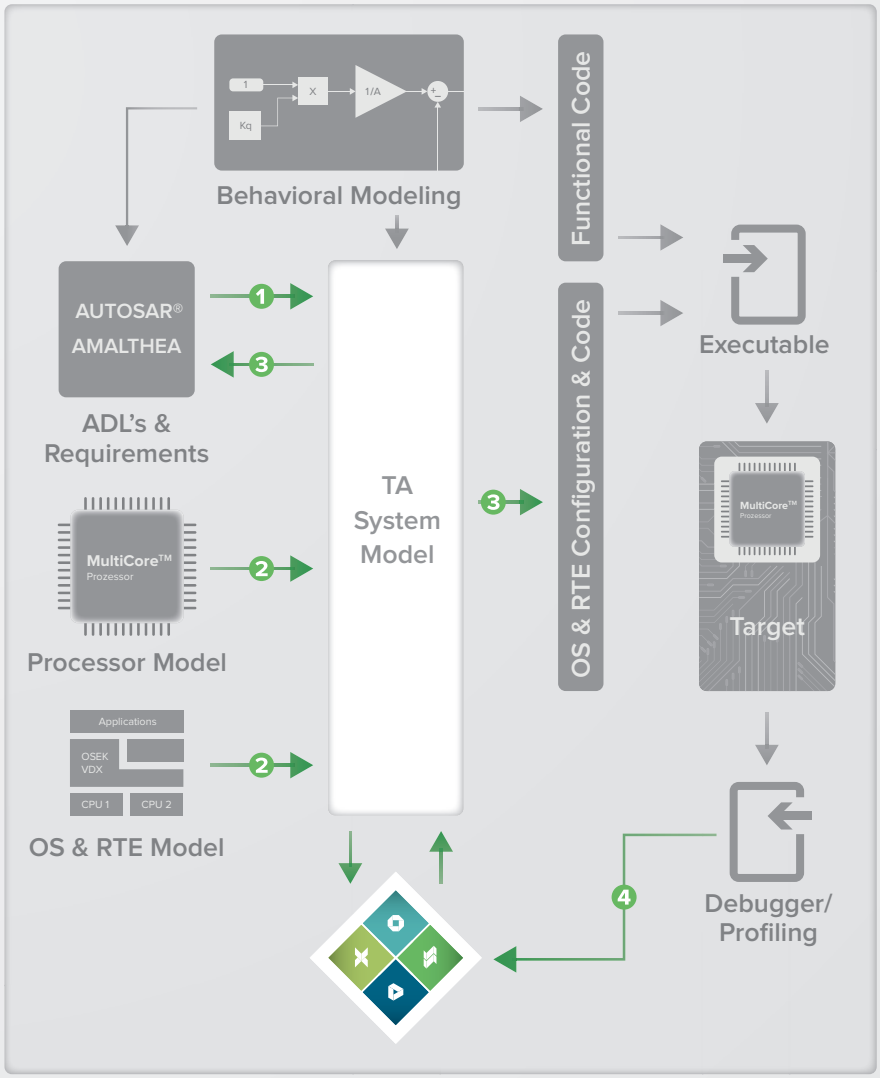
Project Manager	● ●	● ●	● ●	● ●
Software Architect	● ● ●	● ● ●	● ● ●	● ●
Software Developer	● ●	● ● ●	● ●	● ● ●
Integration Engineer	● ●	● ● ●	● ● ●	● ● ●
Test Engineer	●	● ●	●	● ● ●

Timing Architects™ Tool Suite Benefits

The TA Tool Suite allows you the import of AUTOSAR® System Description and/or ECU Configuration files. In standardized development processes, this allows the automation of the modeling steps. Further imports of standardized formats are available and new or in-house formats upon request.

- Model your embedded real-time system with the intuitive graphical model editor or import existing systems from standard interfaces (e.g. AUTOSAR®, AMALHTEA) as well as from hardware target traces.
- Simulate and optimize different system design alternatives at early stages in the development process.
- Optimize your single-core software architecture for high-performance multi- or many-core processor platforms.
- Make well-founded forecasts about the system utilization and dimensioning of the hardware.
- Compare software implementation alternatives and optimize them regarding real-time and performance properties.
- Import hardware target traces of your software, automatically re-construct a timing model from it, analyze the target trace regarding real-time and performance properties and compare the trace to simulation results.

The TA Tool Suite is the closed-loop solution for iterative system design, simulation, automated optimization, and target verification



1. Import of software description, requirements and further information from standard or customer individual architecture description languages
2. For a detailed analysis, TA provides precise models for semiconductor processors and operating systems
3. Export of optimized architecture description and extended requirements to third-party tools for further processing
4. Import of target traces from debugger or instrumentation based profiling

Designer

Managing complexity of highly integrated and functional systems, enabled by seamless switching between individual abstraction layers and implementation layers for requirements, design constraints and system specification.

Use the TA Designer for:

- Specification of hierarchical requirements
- Design of software architectures
- Mapping of software functions to hardware resources
- Integration of new software modules in existing systems

Designer

The TA Designer enables to manage the complexity of highly integrated and functional systems. This is possible by a seamless switch between different levels of abstraction in your functional composition design as well as software architecture design.

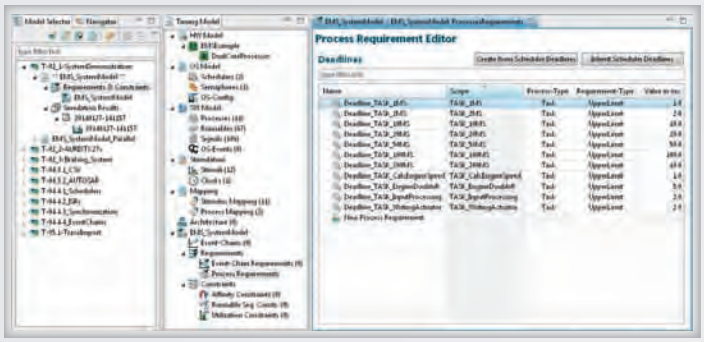
Furthermore, the TA Designer is used for specification of requirements and design constraints as well as integration support tool for internal development and collaborative software development between OEM and Tier 1.

Use the TA Designer for:

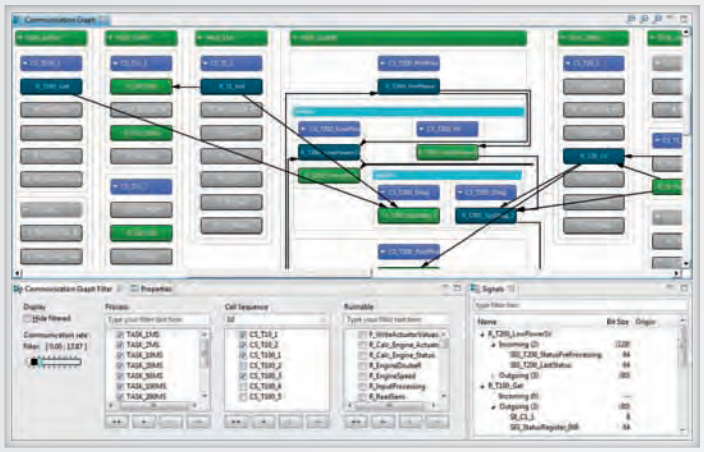
- Functional compositing
- Requirements specification
- Integration of runnables in tasks
- Verification of software architecture constraints
- Exchange of designs in collaborative development

Key-features of the TA Designer:

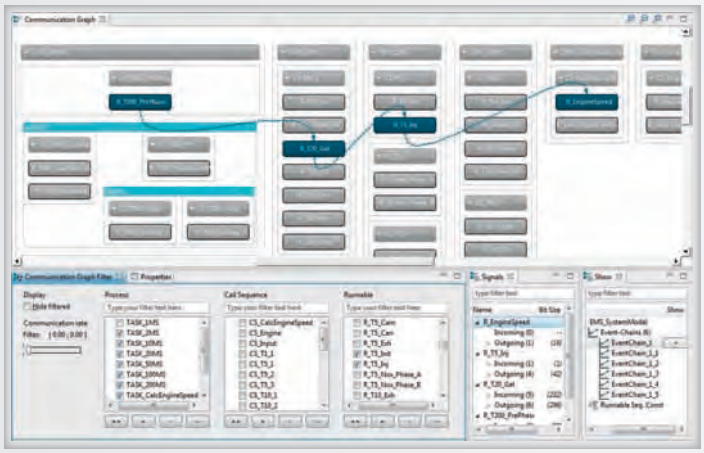
- Support for the system design
  - Various import/export capabilities of software architecture information, e.g. AUTOSAR® or AMALTHEA open-source model, including software components description as well as event-chains and sequencing constraints
  - Automated validation of individual system architecture design constraints
  - Intuitive specification of requirements including timing and resource-consumption requirements
  - Graphical specification of event-chains, e.g. for data-flow evaluation
  - Specification of system architecture constraints, e.g. runnable sequencing constraints
  - Interactive graphical data flow and interaction visualization on all software layers
  - Automated data consistency checking
  - Many views are enhanced by information from simulation, executed in the background, and automated validation checks on the model
  - Interactive UML editing capabilities
- Means to aggregate software in a functional or logical structure to make complexity manageable
- Graphical support for merging different software models and automated consolidation of system artefacts as well as automatic integration of collaborative developed software components



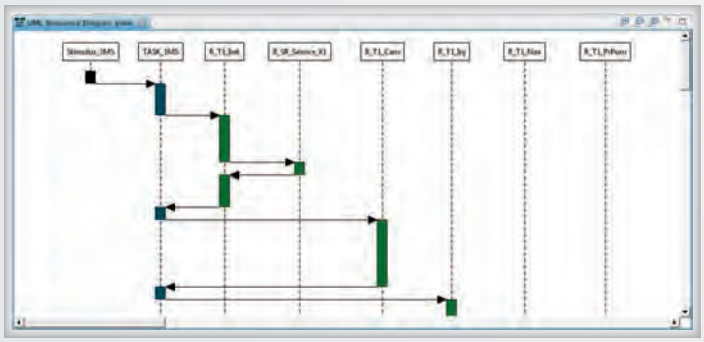
Requirements Specification
Specification of requirements on entity metrics like an upper limit on response time of a task, e.g. deadline, or an upper limit for net execution time of a runnable.



Hierarchical Dataflow Analysis
Interactive hierarchical dependency analysis of the software architecture on all layers, enhanced by advanced filtering and aggregation functions.



Constraints Visualization
Overlay functions allow interactive visualization of requirements and constraints, e.g. event-chains or runnable sequencing constraints.



UML Modeling
Modeling and visualizing the system model with familiar UML diagrams as well as export for documentation purpose and exchange with other stakeholders.

Grouping and Structuring of Software Artefacts
Functional or logical aggregation of software artefacts, e.g. runnables or signals, in order to make complexity manageable.

Simulator

In-depth analysis of system behavior regarding timing behavior and resource efforts, enabled by interactive and interconnected data visualization charts.

Use the TA Simulator for:

- In-depth evaluation of the systems and components timing behavior
- Evaluation of hardware resource consumption of application software and operating system
- Performance analysis and evaluation of different hardware platforms and software designs
- Interference and cause-effect analysis
- Validation and comparison of design decisions early in the development process

Simulator

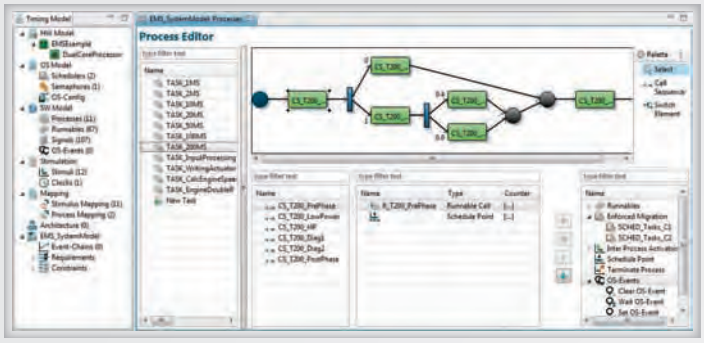
The TA Simulator allows a highly performant simulation and evaluation on scalable abstraction, and detail layers as well as an user-friendly and interactive representation of results. Developed exclusively for multi- and many-core systems, the TA Simulator enables to evaluate system behavior at all stages of the development process. Starting from the early design of the software, without any costly or even non-available hardware, right to the comparison of implementation alternatives. The TA Simulator allows the use of abstract processors, user-designed processors or semiconductor processors, developed by TA in cooperation with chip suppliers.

Use the TA Simulator for:

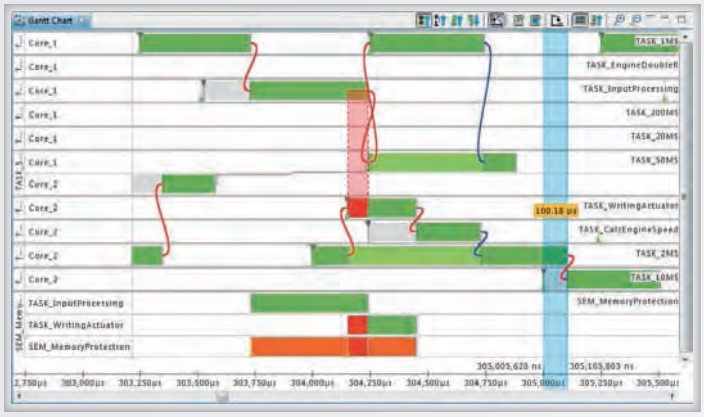
- In-depth evaluation of system and components timing behavior as well as resource consumption
- Evaluating hardware resource consumption of application software and operating system
- Performance analysis and evaluation of different hardware platforms as well as software designs
- Interference and cause-effect analysis
- Validation and comparison of design decisions early in the development process

Key-features of the TA Simulator:

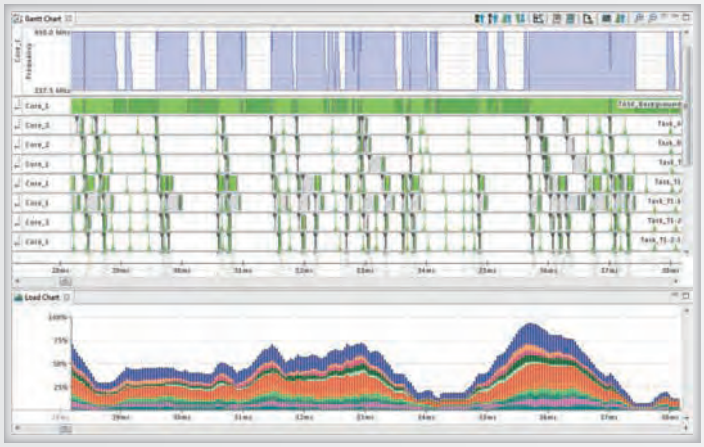
- Model-based schedulability evaluation and comprehensive forecast of the dynamic software behavior of multi- and many-core real-time systems
  - Local and global scheduling, leveraging the full potential of multi-core systems
  - Hardware and software resource consumption and system performance evaluation for multi- and many-core systems
  - Automatic in-depth evaluation of hardware effects, e.g. Cache Hit/Miss, communication overhead or blocking effects
  - Detailed simulation and analysis of abstract or vendor specific processor systems, e.g. Infineon AURIX® or Freescale MPC57xxx family
  - Energy-aware system scheduling analysis (including frequency scaling or core turn-off analysis and visualization)
- Time response evaluations allow a detailed scenario analysis by use of supporting means
  - Metrics and event-chains
  - Requirement violations
- Time, distribution and estimator analysis regarding
  - Temporal resource consumptions
  - Time responses
  - Metrics and event-chains
  - Requirement violations



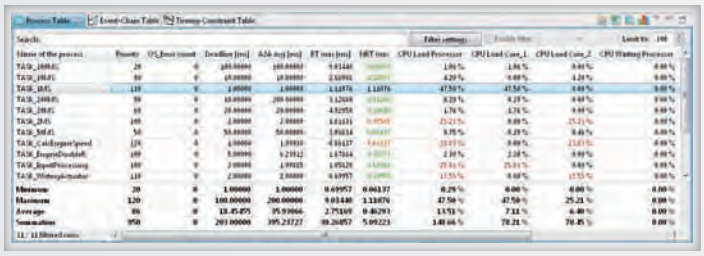
Task Call-Graph Specification
Graphical modeling editor for software model review and interactive modification, e.g. runnable call positions or mode-based branches in task execution path.



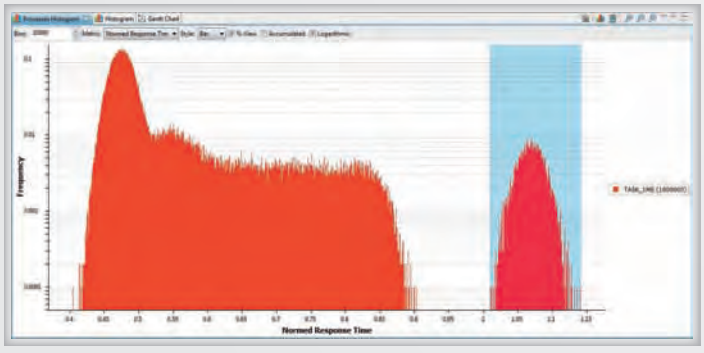
Schedule Sequence
Gantt chart visualization of all traced entities, e.g. tasks, runnables or semaphores, as well as additional status information. This allows analyzing the execution and interaction of software and hardware as well as resource consumption.



Performance Evaluation
Analyzing resource consumption like CPU load as well as effects from dynamic frequency adapting systems as a function of time, in order to improve energy efficiency of the overall system.



Timing and Performance Metrics Evaluation
Overview on metric estimators for all tasks, ISRs or runnables, containing metrics like response time or net execution time with different representative estimators like maximum or average.



Timing and Performance Metrics Distribution
Analyzing the distribution of metrics, e.g. response time, for entity instances on different layers, like tasks, runnables or individual event-chains. The interactive interconnection to other views like the Gantt chart allows an in-depth scenario evaluation.

Optimizer

Semi-automatic software architecture design and deployment of software to hardware, enabled by comprehensive solution comparisons for trade-off analysis.

Use the TA Optimizer for:

- Semi-automated design of embedded multi- and many-core software architectures
- Automated mapping of software functions to hardware resources
- Trade-off and capability analysis of embedded multi- and many-core software architectures as well as hardware platforms

Optimizer

The TA Optimizer allows a model-based design space exploration and automated multi-criteria optimization of embedded systems. Individual needs can be specified and multiple configuration settings can be optimized simultaneously.

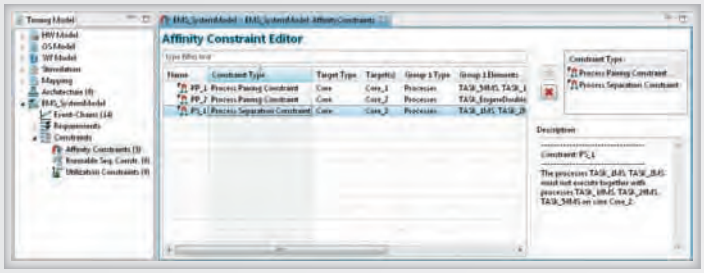
For automatic software deployment on the target platform, TA Optimizer detects automatically sufficient software partitioning and allocation policies. This allows an optimal migration from single- to multi-core systems as well as the improvement of existing multi-core systems.

Use the TA Optimizer for:

- Giving software integrators an objective basis and support at the decision-making process of how to partition and allocate software fragments to individual cores
- Allow software architects to analyze the design space and conduct comprehensive trade-off analysis
- Evaluate different software variations and provide policies to project teams for an optimal multi-core solution over different platforms
- Automatize OS configuration and software deployment

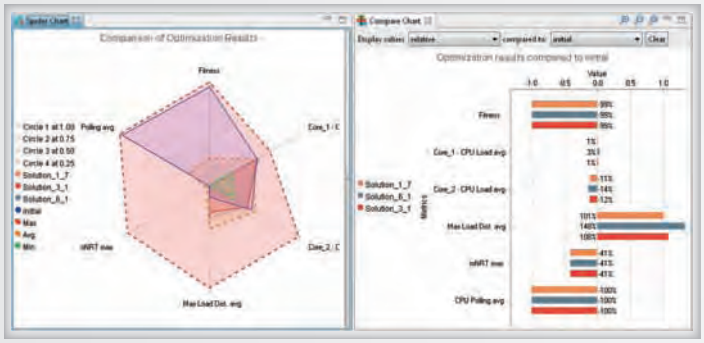
Key-features of the TA Optimizer:

- Automatized optimization of multi-core software architectures regarding specified requirements under consideration of design constraints by improving simultaneously several design decisions
  - Mapping of runnables to tasks
  - Partitioning of tasks
  - Positioning (sequence order) of runnables inside tasks
  - Allocating of tasks to cores
  - Setting of task priorities
  - Setting offset of periodic tasks
- Guided and visualized trade-off analysis of different software designs
- Semi-automated parallelization of single-core software architectures
- Intelligent automatic partitioning (dividing tasks into smaller entities for parallelization and load balancing purposes)
- Automated design-space exploration of timing and system properties of your embedded real-time multi-core system
- Automated detection of software partitioning and allocation policies for software fragments
- Export and update of the OS configuration

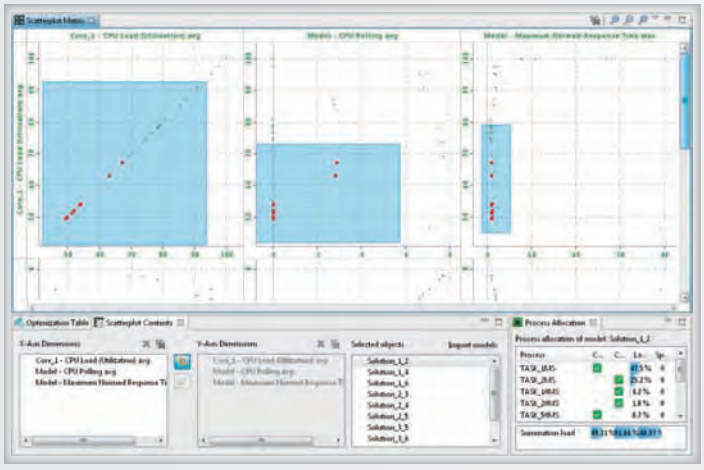


Constraint Specification
Definition of software architecture design constraints, e.g. affinities in the aggregation and positioning of executables or deployment of software to hardware.

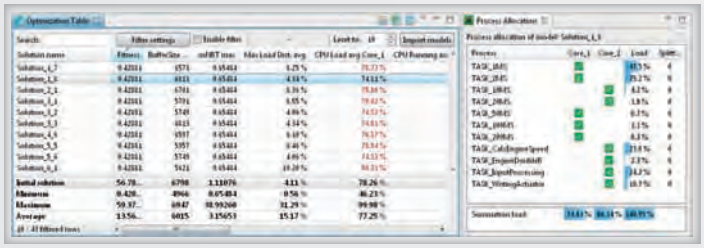
Optimization Configuration
Intuitive configuration of the optimization objectives, allowed system modifications, constraints and requirements as well as optimization search detail level.



Optimization Result Comparison
Comparison of optimized system solutions with initial software architecture or any other solution by benchmarking an individual set of all possible metrics as well as compliance level of requirements.



Trade-Off Analysis
Sophisticated visualization of metrics for multi-criteria decisions and interactive selection of solutions for individual and efficient ranking and selection of the best solution.



Final Solution Selection
Overview on metric estimators for all system metrics and its representative estimators, like maximum, average or minimum, like compact visualization of task and ISR allocation.

Inspector

Verification of real target timing behavior and resource efforts as well as automatic detection of divergence between system model and its software implementation.

Use the TA Inspector for:

- Verification of system implementations on target hardware
- Comparison of system implementations against simulation results and model specification
- Detection of hardware bottlenecks
- Reverse/re-engineering of legacy applications

Inspector

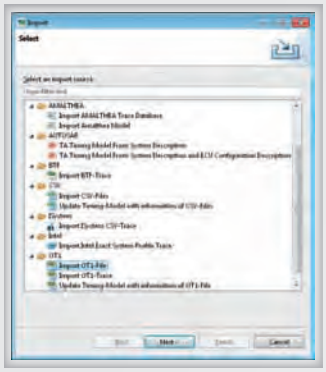
The TA Inspector supports at the verification of real target timing behavior and resource efforts. Furthermore, the TA Inspector supports the automatic detection of divergences between a system model and the generated and executing code on the target. Automatically generated validation reports give project managers and customers easily a precise and automatized status of the delivered products quality.

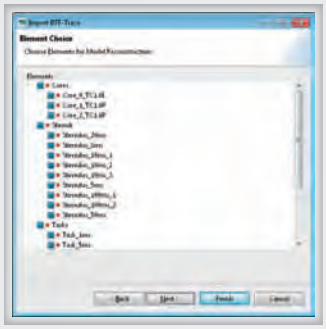
Use the TA Inspector for:

- Automated evaluation of imported hardware traces regarding existing requirements on timing and resource consumption
- Reconstruction of a timing model from a hardware trace
- Fast system health status detection
- Identification of critical scenarios
- Helpful instrument for detecting timing bugs in the application software or operating system

Key-features of the TA Inspector:

- Automatically re-construct a timing model from a real hardware target trace
- Intuitively compare hardware measures with simulation results and therefore, validate the implementation with the simulation
- Import of standard and customer specific hardware traces
- Comprehensive and intuitive visualization of hardware traces
- Validate the hardware trace against specified requirements and generate reports for documentation or project management reporting
- Automatically extract stimulation patterns from imported hardware traces
- Execute time schedule evaluations of the target hardware
- Perform time, distribution, and estimator analysis of target hardware regarding
  - Temporal resource consumption
  - Time responses
  - Metrics and event-chains
  - Requirement violations
- Reverse-engineer application software resource models from hardware traces
- Extract real environment stimulation patterns, e.g. for further use in the TA Simulator



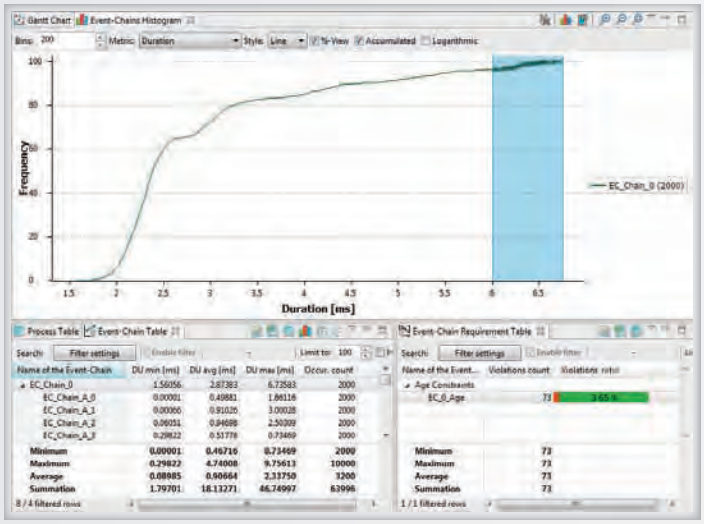


Automated Trace Import and Model Re-construction

Importing target traces and automatically reconstructing a timing model based on individual execution architectures for review or high level evaluation steps.

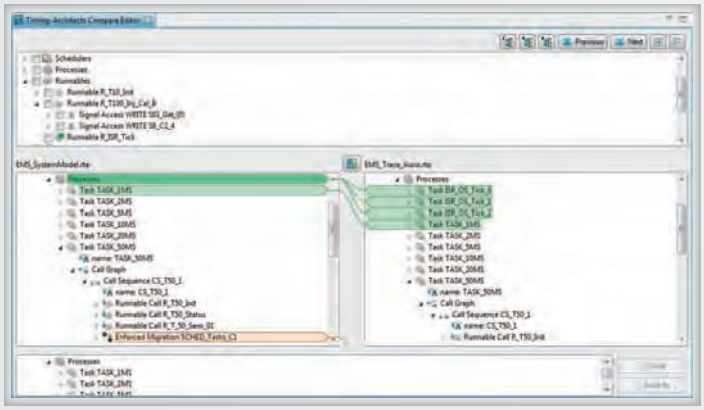
Schedule Sequence

Event-chains and other requirements can be evaluated in the same way as with TA Simulator, simply by copying the requirements specification. This enables the evaluation of the interaction between software and real target hardware as well as an immediate detection of differences between design and implementation.



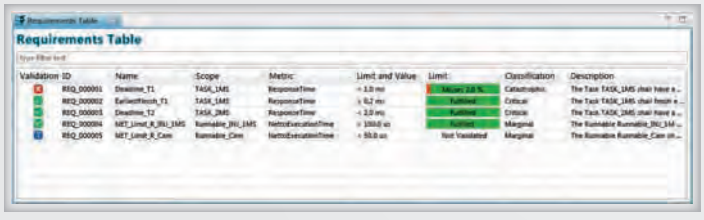
Timing and Performance Metrics Distribution

Analysis of the distribution of metric values on different entities and copying the critical entity instances in order to have a detail analysis.



Automatically check Target against Specification

Detection of divergences between specification and implementation by comparing the automatically generated model of the target trace against the designed system model.



Verification of Requirements

Automatically generated report of verification status on all specified requirements for all kind of entity types giving a fast overview on its compliance/violation ratio. This allows to give project managers and customers a precise status report of the product delivery in a less time-consuming way.

TA Services

Our goal is your successful and efficient multi-core software project.

With Timing-Architects™ Tool Suite we offer user-friendly tools for designing, developing, and verifying embedded multi- and real-time many-core embedded systems.
Our goal is to broaden your performance and increase the efficiency of your product through multi-core technology. TA supports you to extract the true potential of the new multi-core technology. By providing a comprehensive service portfolio, including profound consulting services, broad training offers, and custom software solutions, we make sure, your embedded software solution will perform on the highest possible level.

Consulting

We understand your needs! We are the experts regarding embedded multi-and many-core software architectures. We support you with your multi-core design decisions and assist you in the migration from single-core to multi-core processor system – within all phases of the development cycle. You have not the time or resources to apply our tools to your multi-core project yourself? Our highly trained and motivated experts will assist you in the modeling of your system, the import of your data to our tools, the architecture design, as well as the evaluation and optimization of your embedded real-time system. Together we get the most out of your multi-core system!

Custom Software Solution

With our team of highly skilled and motivated software engineers we provide individual extensions for our tools. We are able to efficiently customize interfaces to integrate with an existing tool chain and development process.
Our development and research departments are also looking forward to new missions, so dare to ask questions and feel free to contact us about your specific multi-core challenge. We are happy to develop your individual software solutions in the area of embedded real-time multi-core systems.

Training

Bring your engineers and developers up to speed on the new multi-core processor technology. We at Timing-Architects™ provide individual trainings and workshops to support your project teams in mastering the multi-core challenge. Our trainings are held by leading experts in the field of multi-core software architectures and embedded real-time systems, and additionally trained in didactic skills. Therfore, we can guarantee you the best support you can get on the market. Besides helping you to develop your multi-core expertise, of course we provide trainings and support for the Timing-Architects™ product portfolio (e.g. how to model an embedded real-time multi-core system with TA Tool Suite and how to evaluate your system with TA Tool Suite).

For more information please feel free to contact us: info@timing-architects.com or +49 (0) 941 604 889 250.

Research Projects

The change from single to multi-core technology in embedded systems results in new challenges, caused by the need to guarantee real-time requirements as well as the efficient use of hardware resources on a highly interacting and interfering hardware architecture.

In order to hold its position as innovation leader in the field of embedded real-time multi-core systems, Timing-Architects™ actively participates in several national and international research projects with university, SME, and industry partners.

- **AMALTHEA** – Model based Open Source development environment for automotive multi-core systems.
- **S³Core** – Design of scheduling algorithms and communication methods for safety-critical multi-core real-time systems, as well as methods for analysis and evaluation of timing-requirements.
- **WEMUCS** – Tools for efficient and iterative development, optimization and test of multi-core software.
- **ZeloS³** – Development of new integrated methods for model-driven design and hardware executed verification for efficient and robust multi-core systems.

Industries

 **Automotive**

 **Mobile**

 **Avionic**

 **Industrial and Medical Automation**

Timing-Architects™ provides leading solutions for the system design, simulation, automated optimization, and target verification of embedded real-time multi-core systems. Our tools and expertise have been proven in many projects in the automotive and mobile devices domain. This gives us deep understanding of the needs and challenges arising with the new multi-core technology.

Most of the techniques and methodologies can be applied out-of-the-box in other domains, like avionic or industrial and medical automation, as well. In some cases domain-specific adaptions may be necessary to fully support the system design or development process or increase precision of simulation. Please feel free to contact us in order to discuss specific requirements of the respective domain.

Automotive

- Motivation for multi-core:
  - More computation power
  - Significantly cheaper (as multiple ECUs)
  - Reducing weight (High-integration of multiple ECUs on one ECU)
- Challenges by applying multi-core:
  - Hard and soft real-time requirements
  - Safety criticality
  - Managing highly collaborative and distributed development (i.e. AUTOSAR®)
  - High variability (generic software is individually configured)

Mobile

- Motivation for multi-core:
  - Integrating co-processors into main-processor
  - More flexibility in dynamic switching between energy saving and performance
  - Reducing reaction time for applications
  - More performance and bandwidth for multimedia applications
- Challenges by applying multi-core:
  - Highly dynamic load requires flexibility of global scheduling
  - Strong mode-dependency in application
  - Saving energy by frequency scaling scheduling algorithms
  - Efficiently manage heavy use of resource locking due to many peripheral interactions

Facing the Multi-Core Challenge

Dear Colleagues,

Embedded systems technology has emerged in many fields of application during the last decades and significantly improved our personal and social productivity, health diagnostic and recovery as well as general comfort in daily life. However, even if embedded systems have made significant improvements in these fields, most systems are far away from fulfilling the criteria what the majority would call adaptive, intelligent or even safe. But, a new fundamental technology has been introduced by semiconductor vendors during the last years, having the potential to deliver enough computation power for highly advanced algorithms and programs – a great possibility and mandatory step for better embedded systems.

For the last three years, Timing-Architects™ has supported several companies all over the world with their first steps applying multi-core technology. We have faced many challenges and have solved many problems together with our customers. We have integrated the insights into our tools and we permanently share our knowledge with our customers and partners, in order to make the start and usage of multi-core technology much easier for them.

Nevertheless, we also know the multi-core development process still has screws for improvement - necessarily we are calling out for an embedded domain mission, the Multi-Core Mission.

Let us revolutionize the system development of embedded systems in a way that multi-core technology becomes not only applicable, but will extraordinary enable to enhance systems function, performance, reliability, and robustness. Let us use the possibility to restructure the development and integrate methodologies and technologies, which have been proven by time to significantly reduce or eliminate unnecessary manual development steps. Performing these inevitable steps, which by now simply were not applied because of the missing need to improve existing legacy repositories. All this is an invest, not to reduce engineer's jobs, but to give space and focus for using our personal capacity in a more valuable way.

In order to follow this Multi-Core Mission, we need you. Facing the Multi-Core Challenge together with us, focusing on new technical question coming up every day with concurrent system development and integrating the insights in our services and tools.
We are looking forward to help you with the migration and successful application of multi- and many-core systems.

Join us and let´s face the Multi-Core Challenge together.

Sincerely,

Dr. Michael Deubzer, CTO

Timing-Architects Embedded Systems GmbH was awarded by the BMWi as Germanys most innovate Start-Up of the year 2011 as well as Germanys new information and technology company of the year 2013.

For more information please contact

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DIN ISO 9001:2008